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Test results judgment method based on BIT faults

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Abstract Built-in-test (BIT) is responsible for equipment fault detection, so the test data correctness directly influences diagnosis results. Equipment suffers all kinds of environment stresses, such as temperature, vibration, and electromagnetic stress. As embedded testing facility, BIT also suffers from these stresses and the interferences/faults are caused, so that the test course is influenced, resulting in incredible results. Therefore it is necessary to monitor test data and judge test failures. Stress monitor and BIT self-diagnosis would redound to BIT reliability, but the existing anti-jamming researches are mainly safeguard design and signal process. This paper focuses on test results monitor and BIT equipment (BITE) failure judge, and a series of improved approaches is proposed. Firstly the stress influences on components are illustrated and the effects on the diagnosis results are summarized. Secondly a composite BIT program is proposed with information integration, and a stress monitor program is given. Thirdly, based on the detailed analysis of system faults and forms of BIT results, the test sequence control method is proposed. It assists BITE failure judge and reduces error probability. Finally the validation cases prove that these approaches enhance credibility.

1. Introduction

Built-in-test (BIT) system is an affiliated part with functions of health management and fault diagnosis.[1,2] Its test course is constituted by electronic components and connectors.[3] The test data is sent to processors and memorizers for operation and storage by transmission path (fiber, cable, bus, etc.), so its correctness relies on BIT equipment (BITE) state. However, testing is interfered by environment stresses, which will even cause the corresponding failures. The wrong test results are direct consequences which cause BIT false alarms and non-detection.[4–7] The data correctness should be guaranteed and BITE failures must be judged, thus the stress monitor program and test sequence control method are proposed to enhance self-diagnosis capacity of BIT system.

The designers prefer protection designs, while BIT improvement methods have been proposed. NASA has been researching on aviation BIT system and indicated that BITE reliability is critical. Certain methods are: continuous monitor, voter,

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chain method, overlap BIT, etc.[8–10] The unsteady operating state and measuring errors cause test errors, so the test data temperately exceeds to cause wrong alarms.[11] For effective maintenance action, false alarm analysis and reduction are necessary.[12] It is acknowledged that most BIT errors derive from data gathering and process and there are many methods to solve this problem, among which Rahman et al. propose a novel framework for sensor data.[13] Allen indicates that BIT itself is a main cause of false alarms and the Bayes theory is an effective solution.[14] The equipment working environment is becoming worse with the wide application and high indexes; Deng et al. think that both of the intermittent fault and the environment stress are main causes of false alarms.[15] The direct consequences are that BITE failures become common, so that the BIT self-diagnosis technology is necessary and essential.

This paper illustrates the consequences influenced by the environment stresses. Then the composite BIT program is summarized and BITE failure judge method is proposed to get correct diagnosis results. The program weakens the stress influences; the stress monitor gives an accessorial judgment for test results; the BIT test results are analyzed and classified for sequence control method. These methods are used in a radar testability improvement project and their efficiencies are proved.

2. Influences of environment stress

Different kinds of stresses are dominant under special conditions: the temperature is difficult to control in upper air and deep sea; the vibration increases with high acceleration and agility; great integration degree makes the electronic components be interfered by electromagnetic stress more easily. The subassemblies of test course are influenced, causing interference/failure, so the test data errors are generated. Fig. 1 shows how the stresses influence testing and result in BITE failures. Then BIT system cannot run successfully and the fault diagnosis results become unreliable.

(1) Temperature stress

The equipment constantly suffers temperature stress during all life time. The typical failure modes include parameter float, sealing failure, component aging, bad contact, etc. For example, the high integrated circuits (IC) work and generated thermo. The heat-collecting phenomenon is obvious to cause these severe failure modes. This stress causes 40% time stress failures.[16–19]

(2) Vibration stress

The main vibration forms are as follows: the connectors suffer vibration with quite higher amplitude; the sympathetic vibration occurs with similar frequencies; fatigue damage is caused by too many vibration circulations. The common failure modes include crack, short circuit, looseness, contact open, etc. It causes 27% time stress failures.[20]

(3) Electromagnetism stress

This stress is acknowledged as a critical factor for electron devices, without concrete statistical data. The typical failure modes include semiconductor puncture, lap joint, false action, short circuit, etc. There are two main consequences: the system would recover with no physical damage; the permanent failures occur with direct damage. For example, the common radiation threshold of semiconductor damage is 10^{-5}–10^{-2} J/cm^2; for the damageable device, it is reduced to 0.1–1.0 μJ/cm^2; for instantaneous failures, the threshold is lowered by 2–3 orders of magnitude.

Fig. 2 shows the high frequency simulator structure (HFSS) simulation model of an electric circuit (multi-chip module, MCM). It is in the cabinet made by aluminum 5A06 and the thickness is 7 mm. Figs. 2(a)–(b) is the HFSS analytical results of the overall and local model separately. The stress concentration is not obvious, the maximum and common values only have about 2 multiple difference.[21] The coupling current mainly enters from pin and line. With coupling electric signals, the MCM cannot work normally.

(4) Analysis of BIT system influences

The stresses influence reliability and performance of BIT system seriously, so that uncertain aftereffects occur and data credibility declines. It is known that: the stress influences BIT results; it causes system and BITE failures; the errors can be weakened but not eliminated. The BIT correctness is defined by test course, feature signals and noise. When the noise grows larger, the output signal fluctuates and test data changes; when there are failures on test course, test data uncertainty occurs.

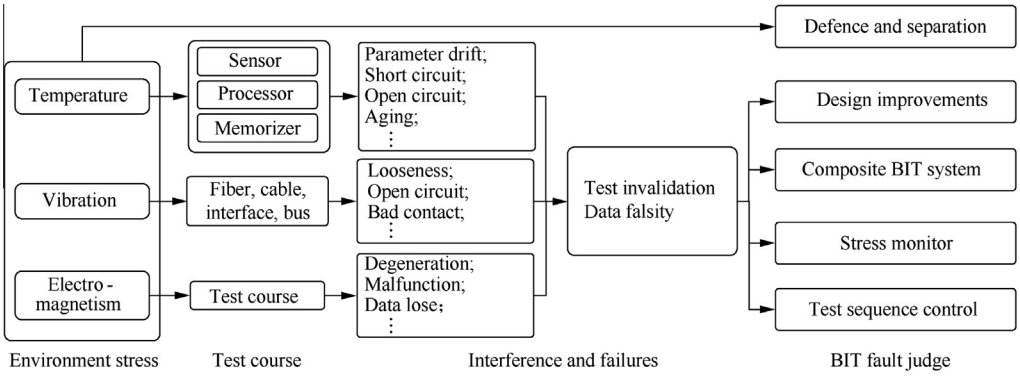
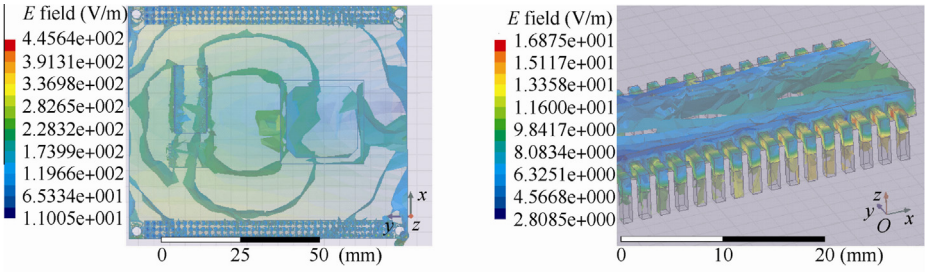


Fig. 1 Illustration of environment influences and corresponding solutions.



(a) Overall electromagnetic field distribution of multi-chip module (MCM)

(b) Electromagnetic field distribution of chip

Fig. 2 HFSS analysis of electromagnetic stress.

Firstly the test data changes temporarily, and then they become unreliable with time and amplitude.

Assume x_r and x_t are real value and test result of fault feature separately and Th is fault alarm threshold. The system healthy probability is that x_r is in normal range, $P(\text{Normal}) = P(x_r < \text{Th})$; BIT pass probability is that x_t is less than Th, $P(\text{Pass}) = P(x_t < \text{Th})$. Because of stress effect and measure errors, they are not equal, $x_r \neq x_t$. So BIT pass does not indicate normal state completely, $P(\text{Pass}) \neq P(\text{Normal})$. BIT no-pass does not equal faulty state, $P(\text{NPass}) \neq P(\text{Fault})$. Then there may be many wrong BIT alarms, most of which would be eliminated by test data process. But some may remain to form BIT false alarms and the effective alarms neglect results in non-detection.

Eqs. (1) and (2) are BIT false alarm rate (FAR) and non-detection rate (NDR). Where, ω indicates BIT pass and $\bar{\omega}$ is BIT alarm, S indicates stress and Δ is the error by test course. FAR is the probability that healthy system is judged faulty, and NDR is the probability that faulty system is judged healthy. The reasons are stress effect and BITE failure.[3] Test credibility would be enhanced with proper diagnosis.

$$\begin{aligned}\text{FAR} &= P(\bar{\omega}|x_t, x_r < \text{Th}) \approx P(x_t > \text{Th}|x_r < \text{Th}) \\ &= P[x_t(S) > \text{Th}|x_r < \text{Th}] + P[(x_t + \Delta) > \text{Th}|x_r < \text{Th}] \quad (1)\end{aligned}$$

$$\begin{aligned}\text{NDR} &= P(\omega|x_t, x_r > \text{Th}) \approx P(x_t < Th|x_r > Th) \\ &= P[x_t(S) < \text{Th}|x_r > \text{Th}] + P[(x_t + \Delta) < \text{Th}|x_r > \text{Th}] \quad (2)\end{aligned}$$

For single test of independent feature, assume that the x_t accords with the normal distribution $R(\mu, \sigma)$ and the cumulative probability function is $\varphi(\text{Th}, k, \sigma)$. Where μ is current feature value, σ is BIT reliability, k is the health point and Th′ is the health critical line. If Th is in $(0, \text{Th}']$, FAR includes two parts: if k is on the left side of Th, $k < \text{Th}$, the false alarm probability is $1 - \varphi(\text{Th}, k, \sigma)$; otherwise, it is $\varphi(k - \text{Th}, 0, \sigma)$. When Th is in $(\text{Th}', 1]$, FAR is completely decided by the probability that $k > \text{Th}$, $\varphi(k - \text{Th}, 0, \sigma)$.

$\text{FAR} = N_{\text{FA}}/(N_{\text{FA}} + N_{\text{D}})$ becomes

$$\text{FAR} = \frac{\int_0^{\text{Th}'} \varphi(k - \text{Th}, 0, \sigma)\mathrm{d}k}{\int_0^{\text{Th}'} \varphi(k - \text{Th}, 0, \sigma)\mathrm{d}k + \int_0^1 \varphi(x - \text{Th}, 0, \sigma)\mathrm{d}k} \quad (3)$$

Similarly, $\text{NDR} = N_{\text{ND}}/(N_{\text{ND}} + N_{\text{D}})$ becomes

$$\text{NDR} = \frac{\int_{\text{Th}'}^1 \varphi(\text{Th} - k, 0, \sigma)\mathrm{d}k}{\int_{\text{Th}'}^1 \varphi(\text{Th} - k, 0, \sigma)\mathrm{d}k + \int_0^1 \varphi(x - \text{Th}, 0, \sigma)\mathrm{d}k} \quad (4)$$

3. Central BIT management

There are some useful testability designs described in introduction. Furthermore a central BIT management can reduce stress influences and advance test data efficiency. It includes the composite BIT program and stress monitor.

3.1. Composite BIT program

By integrating the existing test items and BITE, the composite BIT program is planned on system level. It handles and records test data of (all) periodic BIT and (some) maintenance BIT. They reflect system health state of all life cycle. It includes two parts: all the possible components are integrated for efficiency and protection; the software controls BIT and manages BIT information.

BITE failure rate F_{BIT} is quite lower than the corresponding line-replacement-unit (LRU) failure rate F_{LRU}, and their usual failure rate ratio is $10F_{\text{BIT}} \leqslant F_{\text{LRU}}$. However, BITE is embedded, both failure rate rises and lifting speeds are similar, $\Delta F_{\text{BIT}} \approx \Delta F_{\text{LRU}}$. Then BIT system reliability cannot be guaranteed. All the feeble components are required to be located in an individual part to prevent stress interference. The composite BIT centralizes the process parts and the BIT test points only have data gathering facilities. By effective defense, BITE failure rate rise is lowered, $\Delta F_{\text{BIT}} \ll \Delta F_{\text{LRU}}$. The integrated BIT design needs collectivity design and the cost is higher, but the anti-stress capability is better.

The program diagnoses with historical records and LRU failure rate in the database to locate the fault in size-stated ambiguous group. It contains the modules of BIT control, data gathering, data process, database management and display. An industrialized computer is used to gather and process information. It selects needed test items and gives test requests to related LRU. Fig. 3 depicts how the composition BIT program works. Firstly the BIT data from subsystems is sent to database after decode. Secondly the false alarms are removed with certain rules in database. Thirdly the fault isolation module works with real-time and historical information. Finally the results are presented to users. The diagnosis tree and LRU failure rate are required for isolation. The tree is gained by eXpress, testability engineering and maintenance system (TEAMS), testability analysis, design and evaluation system (TADES) or other software. The test and control module manages test items, responsible for communication with other control subsystem.

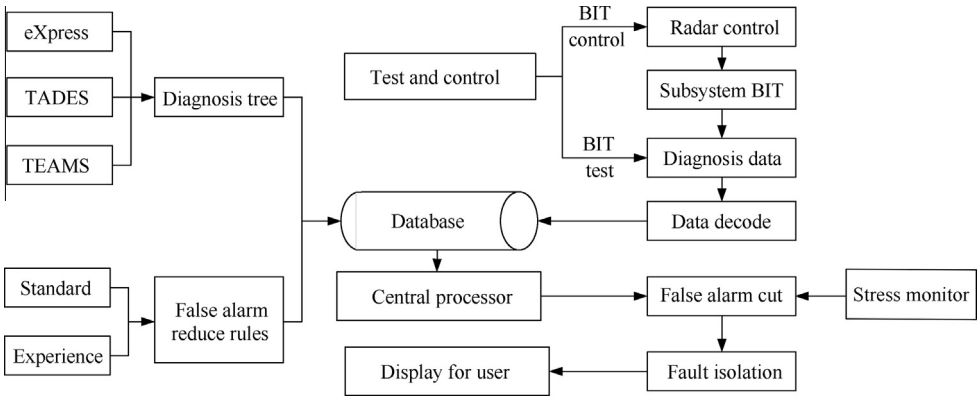


Fig. 3 Flowchart of composite BIT program.

3.2. Stress monitor program

If the stress becomes considerable, the probability of BITE failure grows higher and the test data becomes unbelievable. In Fig. 4, the x-axis denotes the stress, and the y-axis denotes the value of failure rate and health. Their relation is: in the rated area $(0, S_1]$, the failure rate remains at a lower value; with increased stress $(S_1, S_2]$, the system is interfered; in the damage area $(S_2, S_3]$, the damage increases and intermittent faults occur; when it achieves endurable limit $S > S_3$, the permanent faults occur. The interference usually causes data fluctuation and high stress causes the damage.

Therefore, a stress monitor is required to judge testing reliability and its purpose is an elementary judgment. Fig. 3 shows that it helps false alarm cut.

(1) Because the defense capabilities are different, the BIT system failure rate is $F_{\mathrm{BIT}} = \sum_{i=1}^{p} a_i F_i + \sum_{j=1}^{q} b F_j$; a_i and F_i depict defense coefficient and failure rate of i BITE separately; b and F_j depict defense coefficient and failure rate of central BITE separately.

(2) The components' failure rate change with environment stress, and $F_i(S)$ denotes the failure rate with stress S. $F_i(S)$ is gained by relative materials or reliability experiments, whole BITE failure rate is $F_{\mathrm{BIT}}(S) = \sum_{i=1}^{p} a_i F_i(S) + \sum_{j=1}^{q} b F_j(S)$.

(3) Using BIT test credibility to guarantee BIT results, which is 10 times higher than the main system. If BIT health accords with monitor program, the BIT system failure rate is only correlative with test course. Then BIT credibility is

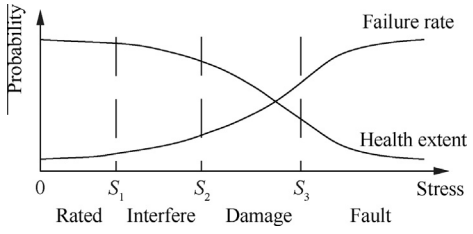


Fig. 4 Relationship between health probability and stress.

$$P(\mathrm{TEST}) = \mu P'_{\mathrm{BIT}}(S) = \mu\left(1 - \sum_{i=1}^{p'} a_i F_i(S) - \sum_{j=1}^{q'} b F_j(S)\right) \quad (5)$$

where $P(\mathrm{TEST})$ indicates BIT credibility, $P'_{\mathrm{BIT}}(S)$ credibility of test course and μ the credibility extent.

(4) If $P(\mathrm{TEST}) > P_{\mathrm{Th}}$, BITE failure probability is lower than credibility. BIT result takes less risk and it is believable.

4. BIT self-diagnosis

4.1. Analysis of test data and fault forms

The basic detection principle of BIT system is to test fault feature and judge whether it exceeds the alarm threshold. Because the maintainers only need binary classification of system running state (normal or faulty), all inconformity results are judged faults. But the fault diagnosis is not so simple. Because the fault conditions may be iterative and the features represent different forms, the forms of faults and test data have various representations too. It may include no signal, continuous or discontinuous excess, error code and unequal value. Both of system and BIT states can be diagnosed exactly based on all the conditions of test data.

Actually the BIT results and main system fault forms are mainly classified into three forms: no-data, unequal, error code. The BIT data forms could show the kind of the system/BITE failures. It helps judge the BIT results correctness by comprehensively analyzing these states. The main system health states are ["normal", "no-data", "unequal", "error code"], whose correspondent symbols are $[0, \emptyset, 1, \Re]$; BIT result forms are ["normal", "no-data", "all normal", "all fault", "error code"], whose correspondent symbols are $[0, \emptyset, \bar{0}, \bar{1}, \Re]$. Assume that the equipment failure rate is λ_{E} and BITE failure rate is λ_{BIT}. $[P_{\mathrm{E}}(0), P_{\mathrm{E}}(\emptyset), P_{\mathrm{E}}(1), P_{\mathrm{E}}(\Re)] = [\alpha, \beta, \gamma, \delta]$, $[P_{\mathrm{B}}(0), P_{\mathrm{B}}(\emptyset), P_{\mathrm{B}}(\bar{0}), P_{\mathrm{B}}(\bar{1}), P_{\mathrm{B}}(\Re)] = [a, b, c, d, e]$, $\beta + \gamma + \delta = \lambda_{\mathrm{E}}$, $b + c + d + e = \lambda_{\mathrm{BIT}}$, $\alpha + \lambda_{\mathrm{E}} = 1$, $a + \lambda_{\mathrm{BIT}} = 1$, $\lambda_{\mathrm{E}} \geqslant 10\lambda_{\mathrm{BIT}}$, $\alpha \gg \lambda_{\mathrm{E}}$, and $a \gg \lambda_{\mathrm{BIT}}$.

Table 1 shows all the test conditions, corresponding probabilities and actual system/BIT state. The basic principles are as follows: when BIT system is normal, the results are believable; it is false alarm with normal main system and abnormal BIT; both faulty probabilities are tiny, but there are many kinds of results, such as wrong result with non-detection and coincident

Table 1 Fault diagnosis probabilities by analyzing test results.

Number	Main system	BIT system	Test result	Diagnosis	Probability	Actual condition
1	0	0	0	0	$\alpha \times a$	Correct result
2	0	Ø	Ø	1	$\alpha \times b$	False alarm
3	0	$\bar{0}$	$\bar{0}$	0	$\alpha \times c$	Correct result, actual non-detection
4	0	$\bar{1}$	$\bar{1}$	1	$\alpha \times d$	False alarm
5	0	$\Re$	$\Re$	1	$\alpha \times e$	False alarm
6	Ø	0	Ø	1	$\beta \times a$	Correct result
7	Ø	Ø	Ø	1	$\beta \times b$	Correct result, actual wrong
8	Ø	$\bar{0}$	$\bar{0}$	0	$\beta \times c$	Wrong result, actual non-detection
9	Ø	$\bar{1}$	$\bar{1}$	1	$\beta \times d$	Correct result, actual wrong
10	Ø	$\Re$	$\Re$	1	$\beta \times e$	Correct result, actual wrong
11	1	0	1	1	$\gamma \times a$	Correct result
12	1	Ø	Ø	1	$\gamma \times b$	Correct result, actual wrong
13	1	$\bar{0}$	$\bar{0}$	0	$\gamma \times c$	Wrong result, actual non-detection
14	1	$\bar{1}$	$\bar{1}$	1	$\gamma \times d$	Correct result, actual wrong
15	1	$\Re$	$\Re$	1	$\gamma \times e$	Correct result, actual wrong
16	$\Re$	0	$\Re$	1	$\delta \times a$	Correct result
17	$\Re$	Ø	Ø	1	$\delta \times b$	Correct result, actual wrong
18	$\Re$	$\bar{0}$	$\bar{0}$	0	$\delta \times c$	Wrong result, actual non-detection
19	$\Re$	$\bar{1}$	$\bar{1}$	1	$\delta \times d$	Correct result, actual wrong
20	$\Re$	$\Re$	$\Re$	1	$\delta \times e$	Correct result, actual wrong

correct result; the max probability is that both of system and BIT are normal, $\alpha \times a$; the consequences are usually wrong with BITE failures. But whether BIT or equipment has faults is still unknown. For example, the main system is normal with abnormal BIT, including $\alpha \times b$, $\alpha \times c$, $\alpha \times d$ and $\alpha \times e$. That may cause BIT false alarm.

If feature fluctuation and test errors are ignored, the false alarm and non-detection are only caused by BITE failures. According to Table 1: Eq. (6) denotes correct diagnosis results by normal BIT; Eq. (7) indicates that BITE failures cause two kinds of false alarms; Eq. (8) is false alarm by wrong location; Eq. (9) is false alarm by wrong detection; Eq. (10) is non-detection.

The diagnosis validity relies on raw data, and the existing methods are prone to give more information. The direct method to guarantee the correctness of the results is that BIT alarms when it has faults. The non-detection caused by BIT "all normal" are eliminated but whether equipment/BIT has faults is unknown, so the test sequence control method is proposed.

$$\mathrm{Corr} = P(\text{Normal BIT}) = (\alpha+\beta+\gamma+\delta)a = a \tag{6}$$

$$\mathrm{FAR} \approx P(x_t > \mathrm{Th} | x_r < \mathrm{Th}) = \mathrm{FAR1} + \mathrm{FAR2} \tag{7}$$

$$\mathrm{FAR1} = P(\text{Faulty BIT}|\text{Faulty BIT}) = (\beta+\gamma+\delta)(b+d+e) \tag{8}$$

$$\mathrm{FAR2} = P(\text{Faulty BIT}|\text{Normal system}) = \sum_{\lambda_{\mathrm{BIT}}} \alpha f(\lambda_{\mathrm{BIT}}) = \alpha(b+d+e) \tag{9}$$

$$\mathrm{NDR} \approx P(x_t < Th | x_r > Th) = P(\text{Faulty BIT}|\text{Faulty system}) \approx (\alpha+\beta+\gamma+\delta)c \tag{10}$$

4.2. Test sequence control method

4.2.1. Testing principle

Actually interference can be classified as temporary failures, so the test results rely on test course. If the environment stress interference is excluded, only BITE failures influence diagnoses. By comparative analysis of test data and system/BIT fault, it is possible to achieve BIT self-diagnosis. If BIT results are defined, whether there are failures of test course could be judged by comparing test results and preconcerted results. The test sequence control method proves feasibility.

The method includes three parts: a series of designated data is produced; BIT results are gained by testing the feature signals; the actual conditions are diagnosed by comparing the results with correct results. These results should contain all the system/BITE failures. The concrete steps are that the test period t is divided into 4 parts, $[t_0, t_1]$, $[t_1, t_2]$, $[t_2, t_3]$ and $[t_3, t_4]$. In $[t_0, t_1]$, there is no input; in $[t_1, t_2]$, the input signal is normal and designated result is "0"; in $[t_2, t_3]$, the input signal is abnormal and the designated result is "1"; in $[t_3, t_4]$, the input signal is practical system signal and the test result is the existing state. Then the test results are $[Ø, 0, 1, V_r]$, V_r is practical BIT test value. If the former 3 parts get correct results, BIT result for main system state is believable; otherwise the BIT system has failures itself.

As Table 2 shows, the test data and results have a corresponding relationship. According to these test data, the BIT results are gained. The test results may have many kinds of permutations and combinations, $4^4 = 256$. However a great number of results are inexistent in practice, such as $[Ø, 0, 0, 1]$. It means BIT result is "no-data" in $[t_0, t_1]$, "normal" in $[t_1, t_2]$ and $[t_2, t_3]$, "faulty" in $[t_3, t_4]$. If BIT has failures that it must give "all normal" persistently, it should not give "faulty" in $[t_3, t_4]$ and the "1" result is a contrary consequence. The main possible test results are shown in Table 2. By comparing actual results, BITE failures could be established.

4.2.2. Testing circuit design

This kind of method is mostly like the combination of active BIT and improved drive signals. It is a kind of method for designated testing and the drive signal is imported to detect the

Table 2 Comparison of test data and BIT results.

Test data	Test result	Problem	Resolution
[Ø, 0, 1, 0][Ø, 0, 1, 1]	Normal BIT, normal system		
[Ø, 0, 0, 0][Ø, 1, 1, 1]	Faulty BIT	Unknown system health state	Offline test
[ℜ, ℜ, ℜ, ℜ][Ø, Ø, Ø, Ø]			
[Ø, ℜ, ℜ, ℜ]	Faulty BIT/system	Whether the system/BIT has faults	Offline test
[Ø, 0, 0, 1]	Inexistent test results		
⋮			

appointed components. Because the drive signal is set beforehand, the results would not be influenced by other component and the environment interference with input signal is weakened. Fig. 5 illustrates the principle of active BIT: system/BIT gives drive signal; the unit under test (UUT) processes these data; the results are tested; test data is compared with settled consequence; the diagnosis conclusion is given to the composite BIT program.

Different from active BIT, test sequence method needs additional BIT performance. As Fig. 6 shows, sequence control and signal adjustment circuit ought to be added before testing. The sequence control part is used for allocating test time, and then the output results and test order are set. The signal adjustment methods include signal multiplication/demulti plication and noise superimposition, so the output results become required signal by signal adjustment. By adding signal adjustment and sequence control module, a series of acquired results is gained.

There are several definition methods of normal and fault signal, the designers must select appropriate one.

(1) The comparison part is based on the tested fault feature value. Even the test item is in a specific range, it could be changed into an upper limit and a lower limit, which is easy to get designated signals.
(2) The multiplication circuit is needed. For example, the normal signal is set 1/2 or 1/3 of real value. If it still cannot meet the normal requirement, then the main system fault extent is severe.

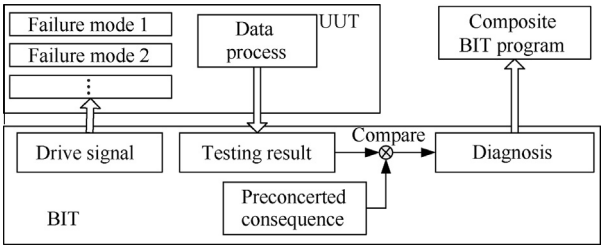


Fig. 5 Principle of active BIT.

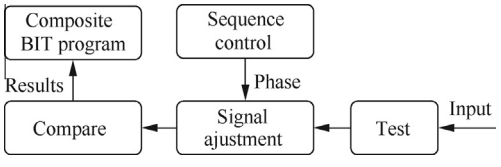


Fig. 6 Circuit diagram design for test sequence design.

(3) The fault value can take noise superimposition to get BITE failure form of "all 1".

5. Validations

Take a radar testability improvement project as an example to validate the methods effectiveness.

(1) Composite BIT program

Fig. 7 indicates the testability design and the broken lines show the improvements. By integrating all possible BIT components and strengthening defense capacity, the stress influence is reduced. By optimizing existing test items and handling all the BIT information synthetically, a composite BIT program is formed. The integrated BIT design gives the hardware better protection. The composite BIT program uses test data more sufficiently and the false alarms are reduced. Based on the theoretical analysis, it can guarantee 90% BITE reliability indexes and reduce 30% false alarms. But the practical application and consequences are still unknown without the users' feedback data.

(2) Stress monitor program

Take electro-static discharge (ESD) effect on certain component as an example. Its fault rate is $\lambda_{\mathrm{E}}^{i} = 8 \times 10^{-6}$ with BITE fault rate $\lambda_{\mathrm{BIT}}^{i} = 7.3 \times 10^{-7}$. Fig. 8 shows the relationship between fault feature and electric stress. In this example, the ordinate is current amplification factor of transistor and the abscissa is ESD voltage. The stress threshold is calculated. Fig. 9 shows boundary by neural network, $S = 700\mathrm{V}$. But BITE failure rate is nearly half of main system

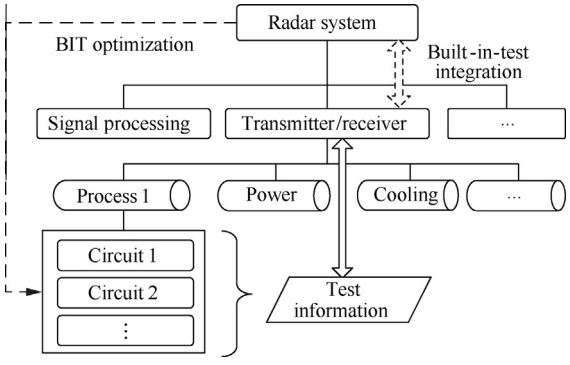


Fig. 7 Radar BIT design improvement.

$0.5\lambda_E^i = 4 \times 10^{-6}$. Actually the BITE failure rate becomes quite high when it exceeds 200V, $\lambda_{BIT}^i \gg 8 \times 10^{-7}$. The BIT results are unbelievable, so stress threshold is directly setting $S > 200$V.

(3) BIT self-diagnosis

Take electrical source voltage test for example. Because each test result is uncertainty, BIT and system failure rates are divided equivalently for various failure forms, $b = c = d = e = 0.25\lambda_{BIT}$, $\beta = \gamma = \delta = 0.33\lambda_E$, $\lambda_{BIT} \geqslant 10\lambda_E$. The steps of test sequence control method are as follows:

(a) The value is required in the range $[Th_l, Th_h]$. It should not be larger than top limit threshold Th_h or smaller than lower limit threshold Th_l.

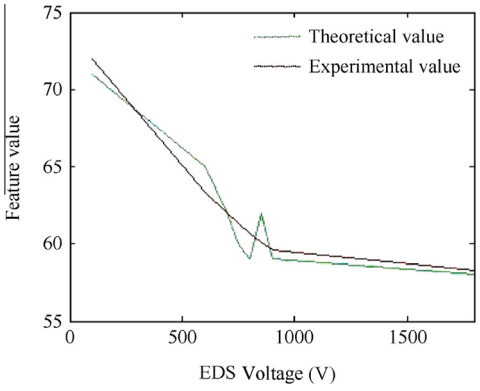


Fig. 8 Relationship curve of feature value and ESD voltage.

Table 3 Comparison of test data and practical condition.

Failure mode	Test data	Practical condition
Voltage fluctuation	[Ø, 0, 1, 0]	Normal system Normal BIT
	[Ø, 0, 1, 1]	Faulty system Normal BIT
	[Ø, 0, 1, 1],[Ø, ℜ, ℜ, ℜ]	Faulty system
	[Ø, Ø, Ø, Ø],[ℜ, ℜ, ℜ, ℜ]	Faulty BIT
	[Ø, Ø, Ø, Ø],[ℜ, ℜ, ℜ, ℜ]	Normal system
	[Ø, 0, 0, 0],[Ø, 1, 1, 1]	Faulty BIT
	[Ø, ℜ, ℜ, ℜ]	Faulty BIT/system

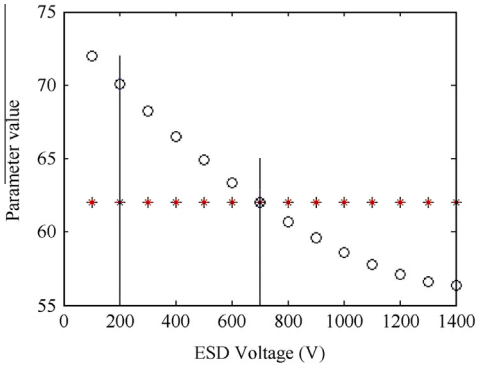


Fig. 9 Test result credibility boundary.

(b) Design test sequence circuit with methods is in Section 4.2.2, including sequence control and signal adjustment.
(c) Use hardware integration method: the comparison circuit is integrated in the main system and sensors are at the signal output location.
(d) Test sequence method is based on comparison of practical conditions and test data presentations.

Table 3 is the comparison of test data forms and practical condition, and then the maintainers could get fault diagnosis results. Where [Ø, ℜ, ℜ, ℜ] means the main system state is "error code", so the multiplication and practical signals are all messy. [Ø, Ø, Ø, Ø], [ℜ, ℜ, ℜ, ℜ], [Ø, 0, 0, 0] and [Ø, 1, 1, 1] represent BITE failures. The offline test is required because the main system health is still unknown.

Assume that all BIT testing results are correct, then the non-detection rate and false alarm rate are reduced. The reduced NDR is $(\alpha + \beta + \gamma + \delta)c = 0.25\lambda_{BIT}$; reduced FAR is $(\alpha + \beta + \gamma + \delta)(b + d + e) = 0.75\lambda_{BIT}$.

(1) Validation results

The methods in this paper are used in the radar testability design and the results are favorable. The improvements avoid wrong test data and the BITE failures are detected to some extent. The composite BIT design makes the BIT hardware get better protection and BIT information more effective. The stress monitor program can generally manage the sensors and simply judge the test data. The test sequence control method manages BIT information comprehensively and gives credible diagnosis results. Table 4 shows several testability improvements.

Table 4 Testability improvements in radar project.

Subsystem	Testing item	Method	Before	After
Frequency resource	Clock signal spectrum test	Active test	Non-detection	Detectable
Transmission/reception	Test of packed received data	BIT hardware integration	Test is unreliable with stress	The defense is effective
Transmission/reception	Test of power temperature	Stress monitor program	The stress is undetectable	Alarm for unreliable data
Signal process	FPGA temperature test	Stress monitor program	The stress is undetectable	Alarm for unreliable data
Array process	Process function test	Test sequence control	BITE failure is undetectable	Alarm for BITE failure
Power	Voltage test	Test sequence control	BITE failure is undetectable	Alarm for BITE failure

Note: FPGA – Field-programmable gate array.

6. Conclusions

By analyzing the influence of stress on electrical components, hardware failures and signal interference are common during test course. Current defense methods could not guarantee BIT reliability, so structure improvement and BIT self-diagnosis technologies are required. A synthesis processing station is established by central BIT management, so the BIT data efficiency is enhanced. Furthermore, the stress monitor is an elementary data judge condition, which can be important supplement of composite BIT program. Based on various equipment/BIT failure forms, the test sequence control method is proposed. Its main value on test anti-jamming is ensuring correct test data. With certain radar BIT improvements, it is proved that the methods could increase BIT diagnosis capacity.

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